_	Name	
	Date	
	Instructor	

EXPERIMENT

Series and Parallel Diode Configurations

OBJECTIVE

To develop the ability to analyze networks with diodes in a series or parallel configuration and to calculate and measure the circuit voltages of various diode circuits.

EQUIPMENT REQUIRED

Instruments

DMM

Components

Resistors

- (1) 1-kΩ
- (2) $2.2-k\Omega$

Diodes

- (2) Silicon
- (1) Germanium

Supplies

DC power supply

EQUIPMENT ISSUED

Item Laboratory serial no.

DC power supply

DMM

RÉSUMÉ OF THEORY

The analysis of circuits with diodes and a DC input requires that the state of the diodes first be determined. For silicon diodes (with a transition voltage or "firing potential" of 0.7 V), the voltage across the diode must be at least 0.7 V with the polarity appearing in Fig. 3.1a for the diode to be in the "on" state. Once the voltage across the diode reaches 0.7 V the diode will turn "on" and have the equivalent of Fig. 3.1b. For $V_D < 0.7$ V or for voltages with the opposite polarity of Fig. 3.1a, the diode can be approximated as an open circuit. For germanium diodes, simply replace the transition voltage by the germanium value of 0.3 V.

In most networks where the applied DC voltage exceeds the transition voltage of the diodes, the state of the diode can usually be determined simply by mentally replacing the diode by a resistor and determining the direction of current through the resistor. If the direction matches the arrowhead of the diode symbol, the diode is in the "on" state, and if the opposite, it is in the "off" state. Once the state is determined, simply replace the diode by the transition voltage or open circuit and analyze the rest of the network.

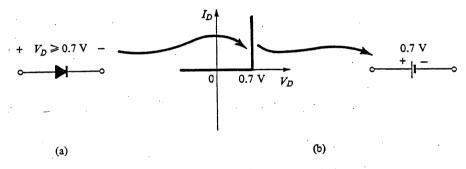


Figure 3-1 Forward-biased silicon diode.

Be continually alert to the location of the output voltage $V_o = V_R = I_R R$. This is particularly helpful in situations where a diode is in an open-circuit condition and the current is zero. For $I_R = 0$, $V_o = V_R = I_R R = 0(R) = 0$ V. In addition, recall that an open circuit can have a voltage across it, but the current is zero. Further, a short circuit has a zero-volt drop across it, but the current is limited only by the external network or limitations of the diode.

The analysis of logic gates requires that one make an assumption about the state of the diodes, determine the various voltage levels, and then determine whether the results violate any basic laws, such as the fact that a point in a network (such as V_o) can have only one voltage level. It is usually helpful to keep in mind that there must be a forward-bias voltage across a diode equal to the transition voltage to turn it "on." Once V_o is determined and no laws are violated with the diodes in their assumed state, a solution to the configuration can be assumed.

PROCEDURE

Part 1. Threshold Voltage V_T

For both the silicon and the germanium diode, determine the threshold using the diode-checking capability of the DMM or a curve tracer. For this experiment the "firing voltages" obtained will establish the equivalent characteristics for each diode appearing in Fig. 3.2. Record the value of V_T

obtained for each diode in Fig. 3.2. If the diode checking capability or curve tracer is unavailable, assume V_T = 0.7 V for silicon and V_T = 0.3 V for germanium.

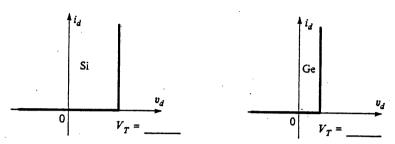


Figure 3-2 Firing voltage for silicon and germanium.

Part 2. Series Configuration

a. Construct the circuit of Fig. 3.3. Record the measured value of R.

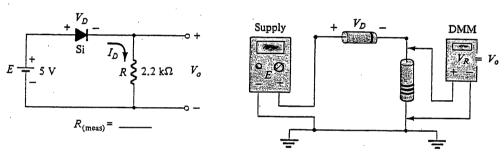


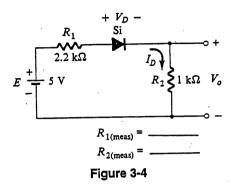
Figure 3-3

b. Using the firing voltages of the silicon and germanium diodes as measured in Part 1 and the measured resistance for R, calculate the theoretical values of V_o and I_D . Insert the level of V_T for V_D .

$V_D =$	
V_o (calculated) =	
I_D (calculated) =	

c. Measure the voltages V_D and V_o , using the DMM. Calculate the current I_D from measured values. Compare with the results of Part 2(b).

d. Construct the circuit of Fig. 3.4. Record the measured values for each resistor.



e. Using the measured values of V_D and V_o from Part 1 and the measured resistance values for R_1 and R_2 , calculate the theoretical values of V_o and I_D . Insert the level of V_T for V_D .

$$V_D = V_o \text{ (calculated)} = I_D \text{ (calculated)} =$$

f. Measure the voltages V_D and V_o , using the DMM. Calculate the current I_D from measured values. Compare with the results of step $2(\mathbf{e})$.

g. Reverse the silicon diode in Fig. 3.4 and calculate the theoretical values of $V_D,\,V_o,\,$ and $I_D.$

V_D =	
V_o (calculated) =	
I_D (calculated) =	

h. Measure V_D and V_o , for the conditions of step 2(h). Calculate the current I_D from measured values. Compare with the results of Part 2(g).

$$V_D$$
 (measured) = V_o (measured) = I_D (from measured) = $\frac{V_o}{R_2}$ = $\frac{1}{R_2}$

i. Construct the network of Fig. 3.5. Record the measured value of R.

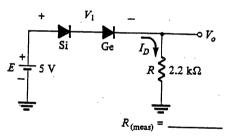


Figure 3-5

j. Using the firing voltages of the silicon and germanium diodes as measured in Part 1, calculate the theoretical values of V_1 (across both diodes), V_o , and I_D .

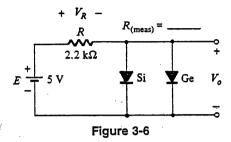
V_1 (calculated) =	
V_o (calculated) =	
I_D (calculated) =	

k. Measure V_1 and V_o , and compare against the results of step $2(\mathbf{j})$ Calculate the current I_D from measured values and compare to the level of Part $2(\mathbf{j})$.

$$V_1 \, ({
m measured}) = \ V_o \, ({
m measured}) = \ I_D \, ({
m from \; measured}) = \ \frac{V_o}{R} = \ \dots$$

Part 3. Parallel Configuration

a. Construct the network of Fig. 3.6. Record the measured value of R.



b. Using the firing voltages of the silicon and geranium diodes as measured in Part 1, calculate the theoretical values of V_o and V_R .

c. Measure V_o and V_R and compare with the results of step 3(b).

$$V_o \text{ (measured)} = V_R \text{ (measured)} =$$

d. Construct the network of Fig. 3.7. Record the measured value of each resistor.

$$R_{1(\text{meas})} = \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ R_1 = 2.2 \text{ k}\Omega \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1} \\ + & & - \\ - & & - \\ \end{array}}_{R_{2(\text{meas})}} + \underbrace{\begin{array}{c} V_{R_1}$$

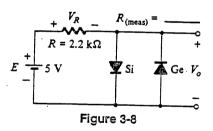
e.	Using the firing voltages of the silicon diode as measured in Part 1, calculate the theoretical values of V_o , V_{R_1} , and I_D .
	$v_0, v_{R_1}, \text{ and } I_D.$

V_o (calculated) =	
V_{R_*} (calculated) =	
I_{R_1} (calculated) = I_D (calculated) =	

f. Measure V_o and V_{R_1} . Using the measured values of V_o and V_{R_1} calculate I_{R_2} and I_{R_1} and determine I_D . Compare to the results of Part 3(e).

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V_o \, ({
m measured}) = \ V_{R_1} \, ({
m measured}) = \ I_D \, ({
m from measured}) =
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g. Construct the network of Fig. 3.8. Record the measured value of the resistor.



h. Using the firing voltages of the silicon and germanium diodes as measured in Part 1, calculate the theoretical values of V_o and V_R .

V_o (calculated) =	
V_R (calculated) =	

i. Measure V_o and V_R and compare with the results of step 3(h).

V_o (measured) =	
V_R (measured) =	

Part 4. Positive Logic AND Gate

a. Construct the network of Fig 3.9. Record the measured value of the resistor.

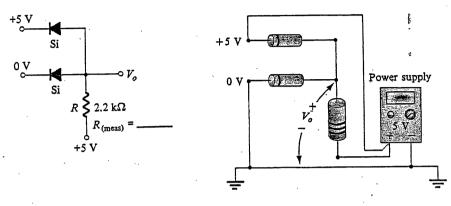


Figure 3-9

b. Using the V_T for both diodes as measured in Part 1, calculate the theoretical value of V_o .

V_o (c	alculated)	=	

c. Measure V_o and compare to step $4(\mathbf{b})$.

$$V_o$$
 (measured) =

d. Apply 5 V to each input terminal of Fig. 3.9 and calculate the theoretical value of V_o .

$$V_o$$
 (calculated) =

e. Measure V_o and compare to the results of step $4(\mathbf{d})$.

$$V_o$$
 (measured) =

f. Set both inputs to zero in Fig. 3.9 (by connecting both inputs to circuit ground) and calculate the theoretical value of V_o .

 V_o (calculated) = g. Measure V_o and compare to the results of step 4(f).

 V_o (measured) =

Part 5. Bridge Configuration

a. Construct the network of Fig. 3.10. Record the measured value of each resistor.

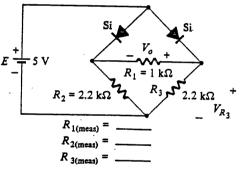


Figure 3-10

b. Using the V_T for both diodes as measured in Part 1, calculate the theoretical value of V_o and V_{R_a} .

 V_o (calculated) = V_{R_3} (calculated) = _____

c. Measure V_o and V_{R_3} and compare to the results of step 5(b). Use a low voltage scale when measuring V_o .

Part 6.	Practical	Exercise
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a. If the diode in the top right branch of Fig. 3.10 was damaged, creating an internal open-circuit, calculate the resulting levels of V_o and V_{R_3} .

 V_o (calculated) = V_{R_3} (calculated) = _____

b. Remove the top right diode from Fig. 3.10 and measure V_o and V_{R_3} . Compare the results with those predicted in Part 6(a).

 $V_o \text{ (measured)} = V_{R_3} \text{ (measured)} =$

Part 7. Computer Exercise

Analyze the network of Fig. 3.4 using PSpice Windows. Compare the results with those obtained in Part 2(f).

 $\begin{array}{lll} \text{Computer } V_o = & & V_o \text{ [Part 2(f)] = } \\ \text{Computer } I_D = & & I_D \text{ [Part 2(f)] = } \\ \end{array}$