The resulting quiescent point from Fig. 7.59 is given by

$$I_{D_Q} = \mathbf{3.4\ mA}$$
$$V_{GS_Q} = \mathbf{1.4\ V}$$

For V_{DS}, Kirchhoff's voltage law results in

$$-I_D R_S + V_{DS} - I_D R_D + V_{DD} = 0$$

and

$$\begin{aligned} V_{DS} &= -V_{DD} + I_D(R_D + R_S) \\ &= -20\ \text{V} + (3.4\ \text{mA})(2.7\ \text{k}\Omega + 1.8\ \text{k}\Omega) \\ &= -20\ \text{V} + 15.3\ \text{V} \\ &= \mathbf{-4.7\ V} \end{aligned}$$

7.14 UNIVERSAL JFET BIAS CURVE

Since the dc solution of a FET configuration requires drawing the transfer curve analysis, a universal curve was developed that can be used for any level of I_{DSS} and universal curve for an *n*-channel JFET or depletion-type MOSFET (for negative V_{GS_Q}) is provided in Fig. 7.60. Note that the horizontal axis is not that of V_{GS} normalized level defined by $V_{GS}/|V_P|$, the $|V_P|$ indicating that only the magnitude of be employed, not its sign. For the vertical axis, the scale is also a normalized level of The result is that when $I_D = I_{DSS}$, the ratio is 1, and when $V_{GS} = V_P$, the ratio V_G -1. Note also that the scale for I_D/I_{DSS} is on the left rather than on the right as enco for I_D in past exercises. The additional two scales on the right need an introduction. tical scale labeled *m* can in itself be used to find the solution to fixed-bias configurati other scale, labeled *M*, is employed along with the *m* scale to find the solution to divider configurations. The scaling for *m* and *M* come from a mathematical deve

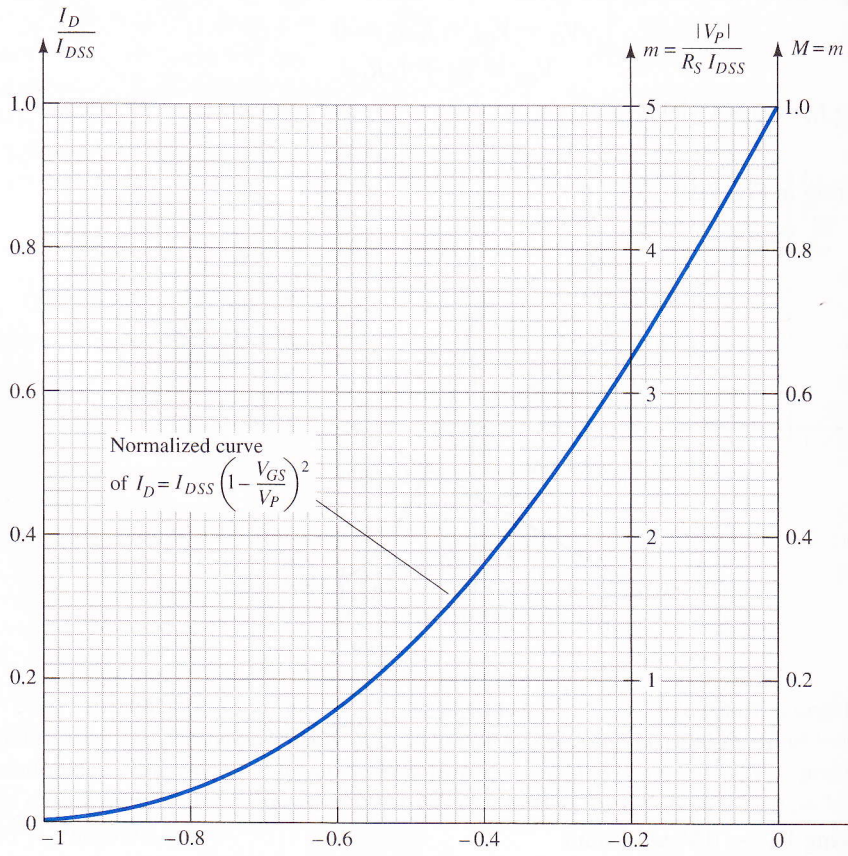

FIG. 7.60
Universal JFET bias curve.